28. (new) The multichip module of Claim 26, wherein said first attach layer is a thermosetting material.

29. (new) The multichip module of Claim 27, wherein said second attach layer is an inorganic material.

30. The multichip module of Claim 26, wherein said first and second chips are approximately the same size.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

The title of the application was objected to as being non-descriptive. The title has been amended in response to the objection.

The drawings were objected to. A proposed amendment to Figure 1 is included herewith.

Claims 1-20 were pending in this application. Non-elected claims 11-20 have been cancelled. New Claims 21-30 have been added.

Claims 1-6 and 8-10 stand rejected under 35 U.S.C. 103(a) as being obvious over Applicant's Admitted Prior Art in view of Takiar, et al. (U.S. Patent No. 5,495,398). Applicant respectfully traverses the rejection. Claim 1 includes the feature of "a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer covering said each of said bonding pads on said first chip and having a thickness to provide electrical disconnection of said first chip wire bonds and

said second chip." Neither Applicant's Admitted Prior Art nor Takiar teach or suggest covering bonding pads with an attach layer. Therefore, Applicant submits that Claim 1 and Claims 2-6 and 8-10 which depend therefrom are patentable over the combined references.

Claim 7 stands rejected under 35 U.S.C. 103(a) as being obvious over Applicant's Admitted Prior Art in view of Takiar and Kuramochi (U.S. Patent No. 5,521,122). Claim 7 depends from Claim 1. Kuramochi does not cure the deficiencies of the combination of Applicant's Admitted Prior Art with Takiar. Therefore, Applicant submits that Claim 7 is patentable over the cited references.

New Claim 21 includes the feature of "a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond, said first attach layer having an area substantially equal to the area of said second chip." The references of record do not teach or suggest such a structure. Therefore, Applicant respectfully submits that new Claim 21 and Claims 22-25 which depend therefrom are patentable over the cited references. Similarly, new Claim 26 includes the feature of "a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip." The references of record do not teach or suggest such a structure. Therefore, Applicant respectfully submits that new Claim 26 and Claims 27-30 which depend therefrom are patentable over the cited references.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-10 and 21-30. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Michael K. Skrehot
Reg. No. 36,682

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
Phone: 972 917-5653
Fax: 972 917-4418

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

WIREBONDED MULTICHIP MODULE [STACKED IC PACKAGE]

In the Claims:

1. (amended) A multichip module comprising:

a first chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a second chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer covering said each of said bonding pads on said first chip and having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip.

21. (new) A multichip module, comprising:

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface;

a wire having a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond, said first attach layer having an area substantially equal to the area of said second chip.

22. (new) The multichip module of Claim 21, further comprising a second attach layer adjacent to said bottom surface of said second chip.

23. (new) The multichip module of Claim 21, wherein said first attach layer is a thermosetting material.

24. (new) The multichip module of Claim 22, wherein said second attach layer is an inorganic material.

25. The multichip module of Claim 21, wherein said first and second chips are approximately the same size.

26. (new) A multichip module, comprising:

a substrate having a plurality of contact pads;

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate;

a wire having a ball bond to one of said plurality of contact pads on said substrate and a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip.

27. (new) The multichip module of Claim 26, further comprising a second attach layer adjacent to said bottom surface of said second chip.

28. (new) The multichip module of Claim 26, wherein said first attach layer is a thermosetting material.

29. (new) The multichip module of Claim 27, wherein said second attach layer is an inorganic material.

30. The multichip module of Claim 26, wherein said first and second chips are approximately the same size.